REMARKS

Applicants acknowledge with appreciation that the arguments filed in the first amendment on November 18, 2003 have been fully considered and were determined by the examiner to be persuasive. Therefore, the rejection has been withdrawn.

To facilitate the examiner's review of the instant amendment, the applicants have set out the various rejections and objections contained in the office action, followed by the applicants' response. The language of the office action is set out in a single spaced and bold format. Each rejection or objection is then followed by the comments of the applicants, presented in double face format.

3. Claims 1 - 2, 9 -10, 12 -19, 26 - 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sfarti, US patent no. 4,809,169 in view of Bitar, US patent no. 5,928,322.

Applicants respectfully submit that the Sfarti patent falls far short of the teachings that are needed to couple the patent with the Bitar patent for an obviousness rejection. Sfarti discloses a coprocessor architecture organized for parallel operation with minimum management support or intervention from a host processor. Preferably, the coprocessors of Sfarti provide for high level graphics oriented management of video display memory planes and video control function associated with the presentation of a video graphic data stream.

4. As to claim 9, Sfarti teaches a network processing system (network, col. 1 lines 20 - 30) including an embedded processor complex for controlling the programmability of a network processor, the complex including a plurality of protocol processor units (PPU), each PPU (computer system 10, col. 5 lines 20 - 30) containing:

at least one core language processor (host processor 12, col. 4 lines, 20 - 30 and fig. 1);

a plurality of coprocessors (coproccssors, 26, 28, 30, col. 2 lines 20 - 50) for executing specific tasks (specific tasks to be performed by each of the multiple parallel coprocessors, col. 10 lines 25 - 30, and col. 1 lines 20 - 25) for the system;

multiple coprocessor interfaces (buses 44, 46, 48, col. 5 lines 30 - 36) to access and share the resources of the coprocessors with each CLP.

Sfarti does not explicitly teach a plurality of protocol processor units, two threads (threads, col. 2 lines 30 - 32).

Bitar teaches two threads (threads, col. 3 lines 60 - 67).

It would have been obvious to apply the teaching of Bitar to Sfarti's system because threads are necessary to run tasks, and implement a plurality of protocol processor units to provide needs for a large network system.

Applicants' invention is now claimed and described as an embedded processor complex that is used for the specific purpose of controlling a network processor and the method of use. The system of applicants is commonly referred to as an MIMD, which refers to a Multiple Instruction-Multiple Data system employing at least two separate instruction streams from each of the core language processors. There is no indication in Sfarti that the patent is suitable or adaptable for the same purpose as intended by applicants. In fact, Sfarti talks about high level graphics-oriented management of video displays. Clearly, this prior art is aimed at an entirely different and distinct market than that of applicants. Furthermore, the system of Sfarti is referred to as a SIMID, or a Single Instruction Multiple Independent Data. As such, it requires no arbiter. Thus, it can be seen that independent claim 9, as now amended, relates to a different system for providing instructions from at least two core language processors to the plurality of specific task coprocessors. On the other hand, Sfarti issues instructions sequentially and, therefore, does not need to arbitrate the sequence in which they are delivered.

Accordingly, claim 9 as now worded is clearly and patentably distinguishable over Sfarti. Applicants specifically indicate there are at least two core language processors and that two arbiters provide an interface between the core language

processors and the various specific function coprocessors. Furthermore, Bitar provides no teaching that would serve to overcome this shortcoming of Sfarti. The fact that Bitar refers to two threads has absolutely no bearing on applicants' claim 9 which specifically states that the two threads are code threads and that they are an integral part of each of the core language processors. Even with the incorporation of the teachings of Bitar into the teachings of Sfarti, the combination falls woefully short of suggesting that applicants' invention as now covered in claim 9 is obvious.

Accordingly, applicants respectfully submit that the newly reworded claim 9 is patentably distinguishable over the combination of the two references, and that the rejection should be withdrawn.

5. As to claim 10, Sfarti modified by Bitar teaches the coprocessor interfaces are dedicated to supporting the code threads of each CLP (coprocessor interfaces are used to interface between processor and coprocessors, so it has to support the threads).

Claim 10 now depends from a newly amended independent claim 9 and, therefore, includes all of the elements thereof. Accordingly, the dedicated coprocessors of claim 10 support at least two core language processors, through two distinct arbiters. These claimed features are not noted in either of the two references. For this reason, the rejection should be withdrawn.

6. As to claim 12, 13, 14, Sfarti teaches the network processing system of claim 10 further including a FIFO buffer (buffer, col. 4 lines 55 - 60) between each thread and at least one of the coprocessors.

Claims 12-14 do specify the use of a FIFO buffer between the two core language processors and the coprocessors. However, any reference to buffers by Sfarti is merely ancillary to the function of his system as a SIMID, and not as a multiple instruction-

multiple data system. Coupled with the substantive changes that applicants have made in the independent claim 9 from which these claims 12-14 depend, applicants respectfully submit that the subject matter of these dependent claims is patentably distinguishable over Sfarti itself and/or in combination with Bitar.

7. As to claim 15, 16, Sfarti teaches the network processing system including specific operating instructions (instructions, col. 5 lines 30 - col. 6 lines 45) executed by the threads of the CLPs which result in commands to control coprocessor operation, which commands flow through the interface between the CLPs and the coprocessors.

Again, with the amendment to independent claim 9 from which claims 15 and 16 depend, applicants respectfully submit that these two dependent claims are allowable. To reiterate, claim 9 now includes at least two core language processors, with a pair of arbiters between the CLPs and the various coprocessors. This feature is nowhere shown in either of the applied references; therefore, the further limitation of claims 15 and 16 in combination with the limitations of claim 9 are neither shown nor inferred.

8. As to claim 17, Sfarti modified by Bitar teaches the network processing system according to claim 15 wherein the instructions enable the system to identify long latency events (latency, col. 4 lines 55 - 67) and short latency events (low-latency, col. 3 lines 59 - 60) according to the expected response time to access data in response to a particular coprocessor command, and to grant full control to another thread when execution of an active thread stalls due to a long latency event, or to grant temporary control to another thread when execution of an active thread stalls due to a short latency event.

Again, with the amendment to independent claim 9 from which claim 17 indirectly depends, applicants respectfully submit that this dependent claim is allowable. Bitar discusses latency but does not describe the identification of long and short latency events and the granting either of full or temporary control to another thread, based on whether the latency is long or short. Furthermore, there is absolutely no clear

understanding as to how the latency dispatching feature of Bitar could be used to any advantage by Sfarti who uses parallel operation for the coprocessors to respond to the host processor. In addition, neither of the references identifies short or long latency events to grant temporary control or full control from one thread to another thread.

Again, the differences between the combination of references and the claimed subject matter of claim 17 point to the allowability of claim 17, particularly when taken in light of the substantive amendments to independent claim 9.

9. As to claims 1 and 18, see claim 9 above.

10. As to claims 2, 19, see claim 10 above.

11. As to claims 26, 27, see claims 15, 16 above.

Applicants have now made substantially the same amendments to independent claims 1 and 18 as were made to independent claim 9. Accordingly, these method claims should be considered as claiming patentable subject matter for the same reasons as presented above. Both of the claims now feature 2 arbiters between the core language processors and the specific function coprocessors.

12. As to claim 28, Sfarti teaches the method according to claim 27 wherein the execution is either direct or indirect (instructions fan be executed in two selectable modes, col. 5 lines 30 - col. 6 lines 45).

Applicants respectfully submit that the direct or indirect execution is not suggested or implied by the teachings of Sfarti. This claim 28 depends from claim 27 which depends from claim 26 and enables conditional execution of coprocessor operation. As now amended, claim 26 depends from claim 21 rather than claim 18, specifying that the direct or indirect execution is arbitrated by the coprocessor execution

interface arbiter. This serves to further differentiate claim 28 and its teachings from the teachings of Sfarti. Accordingly, claim 28 should now be considered to be allowable.

13. As to claim 29, see claim 17 above.

Applicants respectfully submit that this dependent claim is allowable for the same reasons as claim 17. Bitar discusses latency but does not describe the identification of long and short latency events and the granting either of full or temporary control to another thread, based on whether the latency is long or short. As previously noted, there is absolutely no clear understanding as to how the latency dispatching feature of Bitar could be used to any advantage by Sfarti which uses parallel operation for the coprocessors to respond to the host processor. Again, neither of the references identifies short or long latency events to grant temporary control or full control to another thread. Accordingly, claim 29 should be determined to be allowable.

14. Claims 3 - 8, 11, 20 - 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sfarti, US patent no. 4,809,169 in view of Bitar, US patent no. 6,016,542, and further in view of Chung, US patent no. 5,404,469.

Applicants respectfully submit that all of these claims are distinguishable over the combination of references applied by the examiner under §103(a), particularly when considered in light of the revisions made in the three independent claims.

15. As to claim 3, 11, 20, Sfarti teaches checksum coprocessor (numerical data computations, col. 25 - 35).

Sfarti and Bitar do not explicitly teach the coprocessors are selected from the group including a tree search coprocessor, stringcopy coprocessor, enqueue coprocessor, datastore coprocessor, CAB coprocessor, counter coprocessor and policy coprocessor.

Chung teaches datastore coprocessor (load/store unit). Stringcopy coprocessor, counter processor are generic coprocessors executing specific tasks.

It would have been obvious to apply the teaching of Chung to Sfarti's and Bitar's system becaus it provides the design choices for the coprocessors for executing different specific tasks as needed for the system.

Applicants respectfully submit that the addition of Chung to the teachings of the prior art do not alter the fact that the invention as now claimed is patentably distinct over the applied references. Chung merely adds certain specific coprocessors, all of which are well known in the art. However, Chung does not teach or suggest that the incorporation of datastore, stringcopy or counter processors into the system of Sfarti is somehow going to enhance the ability of the principal reference to provide for high level graphics oriented management of video display memory planes and video control function associated with the presentation of a video graphic data stream. Furthermore, there is no suggestion in any of the references that points to such a combination. Accordingly, claims 3, 11 and 20, all depending from claims that have now been shown to be distinguishable over the cited prior art, should likewise be considered to be allowable.

16. As to claim 4, 5, 21, 22, Bitar teaches in the operation according to claim 3 further including a coprocessor execution interface arbiter to determine the priority between multiple data threads (changes to the priority of one or more real-time threads is another event, col. 4 lines 5 - 20).

As pointed out above, the claims from which claims 4, 5, 21 and 22 depend all specify the use of two arbiters between each of the two core language processors and the coprocessors. This feature definitely is not described in Bitar and, accordingly, is not available as a teaching that can be incorporated into the teaching of Sfarti. For this reason, these dependent claims should be considered to be allowable.

17. As to claim 6 - 8, 23 - 25, see claim 12 - 14 above.

Applicants again call the attention of the examiner to the arguments that the applicants submitted *supra* concerning the basis for overturning the rejection of claims 12-14. Because of the differences between a SIMD and that of an MIMD, the operation of the Sfarti invention differs substantively from that of the present invention as now claimed. These same factors that distinguish claims 12–14 over the prior art are applicable to the rejection of claims 6-8 and 23-25. Accordingly, this rejection should be withdrawn.

CONCLUSION

Applicants respectfully submit that all necessary corrections have been made to the specification to overcome the Section 112 issues. Furthermore, they have presented arguments that are sufficient to refute the contention by the examiner that the claims of the present application do not cover patentable subject matter. The principal reference, Chung et al, is prior art, but the relevance of the patent to the claimed subject matter is remote at best. Accordingly, applicants respectfully request that the examiner reconsider his position concerning patentability and withdraw his rejections.

Respectfully submitted,

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